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A Memory Implicit Self-Reconditioning Based On Configuarable Substitutes

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Abstract

We present an MISR generator which automatically generates register transfer level MISR circuits for SoC designers. There is growing need for ingrained memory implicit self reconditioning system (MISR) due to the introduction of more and more system-on-chip (SoC) and other highly integrated products, for memories, and repairing embedded memories by Conventional off-chip schemes is expensive .The MISR circuit has a scalable architecture, and it implements an enhanced version of our EP algorithm for efficient 2-D repair .A typical BISR draft requires circuit modules that perform built-in self-test (BIST), implicit redundancy analysis (IRA), real-time address remapping, and so on. The faulty cells can be repaired immediately after manufacturing but still unused substitutes can serve for replacement during lifetime of systems on chip making them more fault-tolerant.the repair process based testing outcomes and on the repair analysis is done by external devices or by internal blocks integrated directly on chips. The proposed MISR circuit is small, and it supports at-speed test without timing-penalty during normal operation. With its low overhead and zero test-time penalty, the MISR can easily be applied to multiple memories with a distributed RA scheme.

Keywords: Implicit Reconditioning, BIST, EP, SOC, Configuarable Substitutes.

Introduction

There is growing need for embedded Memory implicit self reconditioning (MISR) draft due to the introduction of more and more system-on-chip (SoC) and other highly integrated products, for memories, and repairing embedded memories by Conventional off-chip schemes is expensive[1]. Therefore, a circuit developed MISR generator which automatically generates register transfer level MISR circuits for SoC designers. The MISR circuit is based on a Redundancy Analysis (RA) algorithm that enhances the essential pivoting algorithm, with a more flexible substitute's architecture, which can configure the exact substitute to a row, a column, or a rectangle to fit failure patterns more efficiently. Feature of memory elements is that which in the manufacturing and operation processes of them some cells under the influence of failures can go out of functioning state. But given circumstance not always brings memory element to critical or extreme state, when reconditioning is impossible. At that it is considered such technical state of object, when total quantity of faulty cells does not exceed reserve repair resources. Modern tendencies of semiconductorindustry development involve permanent decrease of silicon chip area It is important to make the distinction between a physical defect in a RAM and a memory failure. A physical defect is anything within the physical structure that deviates from what was intended, such as the presence of unwanted material, the absence of desired material, and imperfections in the lattice of the substrate. A physical defect may or may not lead to a failure, a situation in which the device behaves in such a way that violates its specifications. Physical defects that are not serious enough to immediately cause failure are known as latent defects. Latent defects may worsen with time and eventually reach the point where they do cause failure. Incorrect behavior is described at some convenient level of abstraction as a fault. Faults with similar behaviors are grouped into fault types, and a set of faults that supposedly describes all types of faulty behaviors is known as a fault model. Memory fault models are significantly different than the fault models used for digital logic. Detecting sensitive faults can be very difficult. Developed repair allocations algorithm are based on analysis of a global (or local) failure bit map created during the testing process and the memory substitute allocation has to be done after finishing the whole memory test The result of any repair allocation algorithm is a relationship between the addresses of faulty memory elements and the substitute elements available for repairing the diagnosed faults. The objective of this study is to integrate the implicit recondition analysis together with a repair technique into the chip using BIST, block for replacing the fault module and multiplexers for choosing between main memory and substitute memory and a SRAM main memory. The rest of the paper is organized as follows. System function explained in section II.memory remapping in shown in

section III, Overview of the algorithm is dealt in section IV, Experimental results are presented in section V. Concluding remarks are given in section VI.

System Function (Memory Remapping)

The proposed MISR generator targets large memories (embedded or stand-alone) that require redundancy repair. It takes the memory specification and then generates the RTL MISR circuit, which is a logic circuit that can be synthesized (i.e., converted to a gate-level circuit) using a commercial tool. The MISR circuit has a scalable architecture, and it implements an enhanced version of our EP algorithm for efficient 2-D repair. There is no test time overhead and only a little logic area overhead.

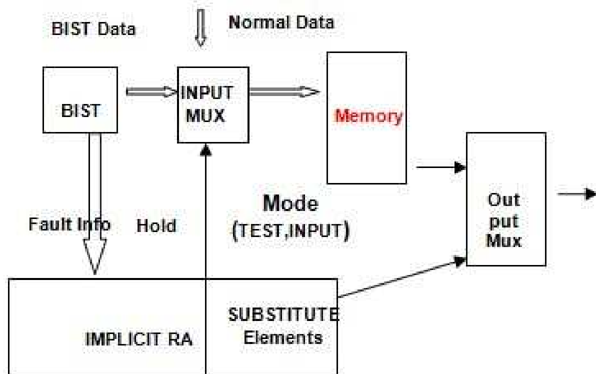


Figure 1. Diagram of MISR using Substitute elements

As in figure the tester controls the MBIST for field reset-triggered repair, the MBIST executes the default March-CW test algorithm after each reset, by connecting some control pins (Ctrl) to VDD or ground. The main memory under test/repair has its own memory substitute. All the memory inputs have multiplexers in front of them to select (use the mode signal) between the normal access channels (in normal mode: INPUTS=CE, D, A, WE) or MBIST channels (in test mode: INPUTS= CETest, DTest, ATest, and WETest). During RA, the MIRA first records the unusable faulty memory substitute elements and then allocates memory substitute elements according to the faulty rows/columns of the main memory based on the test result. When the memory substitute elements are not enough for repairing the faults, the Go signal is de-asserted to abort the MBIST. Otherwise, when the test is done, the Ready and Go signals are asserted. Whenever the MBIST begins testing, the MIRA starts the RA process by detecting the Mode signal. During RA, the MIRA checks the 2-bit Detect M/S signals in the MBIST for the main and memory substitute memory faults, respectively, and analyzes each faulty address from A Fail within the same clock period. In the normal mode, the MIRA remaps the faulty main memory addresses to those of the memory substitute memory that have been determined during the RA process.

A.Logical Pivoting and Configurable Memory substitute Remapping:

Traditional 2-D redundancy repair uses two substitute memory cores for memory substitute rows and columns. However, the pivoting memory substitute remapping uses only one substitute memory core that can remap either a faulty row or column to the same memory substitute element. The memory substitute utilization efficiency increases and area overhead is reduced, as the traditional method requires two different substitute memory cores for columns and rows, respectively, which results in higher area overhead of MBIST and peripheral circuits Furthermore, the logic address is configurable so that the memory substitute element can be mapped from a rectangle or even a set of rectangles to block-repair cluster faults or other special cases. It gives simple conceptual cases showing the strategies of address remapping from various rectangular patterns in the main memory to the memory substitute elements in the memory substitute memory.

The following analysis can be explained by taking an example

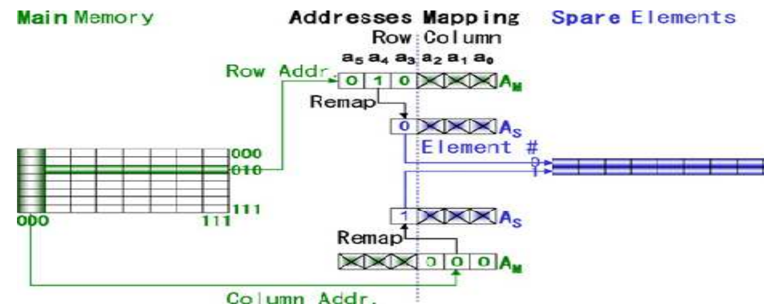


Fig 2 Adress mapping

Fig.2 shows two basic cases when the row and column address lengths of the main memory are equal, the memory substitute row or column elements (from the memory substitute memory) are suitable for repairing the faulty rows or columns. However, because the memory is usually square or close to square, an element might not exactly be a row or column, but just of the same size divided by the most significant bit (MSB) or any address bit[2]. For example, to remap the faulty row (010), the row address ($a_5a_4a_3$:010) of the main memory address (A_M) is remapped to a memory substitute element number (a_3: 0) of the memory substitute memory address(A_S) by the MIRA according to the redundancy analysis results. The other address field ($a_2a_1a_0$) of A_M is the column address, which is don't-care in redundancy analysis, while the same address value will be rearranged to the column address field of A_S during remapping.

Overview of the Algorithm

Fig.3 is an EP example with threshold 2, two substitute rows, and two substitute columns, where rows 1, 5, 6, and column 5 are essential-repair lines, and cell (5, 5) has an orthogonal fault. Due to the lack of a substitute row for the essential-repair row 6, this case will fail during the substitute allocation phase, which allocates substitute rows, columns, or both to specific table items after testing. Fig.3.6 has the same faults as in Fig.3.5, but now each substitute element can be used to replace a faulty row or a faulty column. Therefore, the faults become repairable. Every substitute is initially in the default configuration and configured to repair a row/column when one of the address-coordinates is marked as an essential-repair row/column.

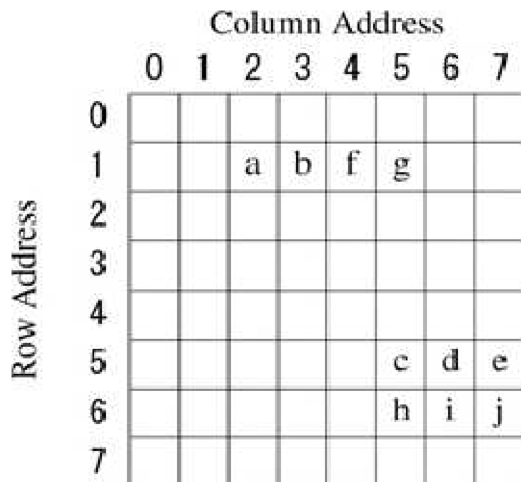


Fig. 2 Memory block with defect sequence.

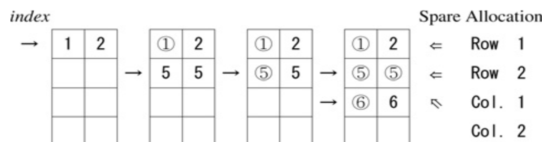


Fig. 3.EP with threshold 2, two substitute rows, and two substitute(spare) columns.

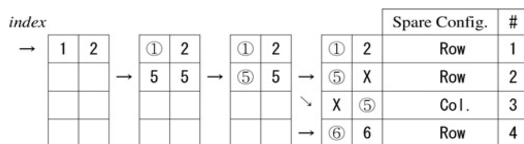
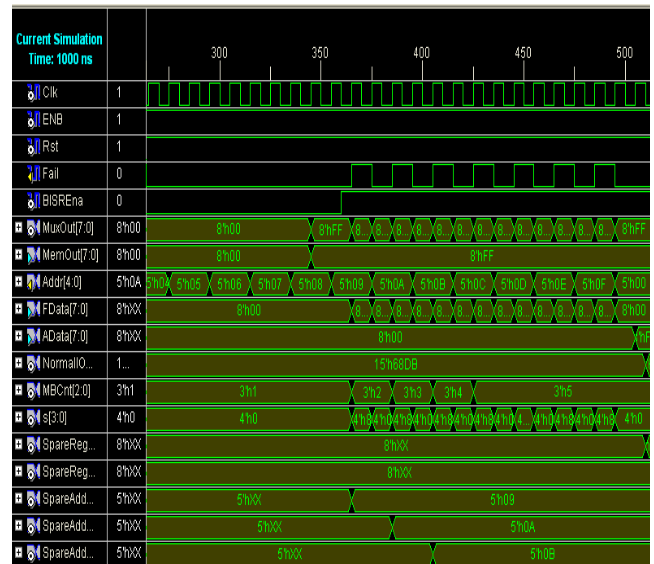


Fig. 4. EP with threshold 2 and 4 pivoting substitute(spare) elements.

For example, Substitutes 1, 2, and 4 are configured as rows, and Substitute 3 is configured as a column when their essential-repair flags (circles) are set. Determination of default configuration depends on the memory structure and failure diagnosis. If an address is marked simultaneously as an essential-repair row and an essential-repair column [e.g., address (5, 5) in Fig.. 8], the address is split into two items (e.g., substitute 2 and 3 in Fig.3.4, where "X" means don't-care) to avoid configuration conflict of the substitute. Because the number of items equals the number of substitutes, the table of the original ESP can have more faults than it can repair. Note that the proposed RA algorithm uses the same table space as the original ESP, and both algorithms use the same memory space for the substitutes. Therefore, the early-abort feature of the proposed architecture has no extra overhead so far as memory space is concerned, while the original ESP needs additional logic for handling the above case, or it fails at the final substitute allocation phase as the substitutes are not configurable[3]. For example, if there is one substitute column available, it cannot repair a faulty row, but the proposed method will reconFig.ure the substitute into a row, so the faulty line can be repaired. Therefore, the repair rate improvement depends on the fault distribution. Consequently, with the proposed algorithm, the substitute allocation phase can be omitted to simplify the MISR, i.e., with lower area. Moreover, the two components of a general MBISR, i.e., the MIRA, for RA, and address remapping unit [(ARU) for normal mode] can be easily merged to share the area-dominating CAM or address-comparators and registers.

Result

The below figures shows the overall simulation results in top module where all the modules like mbist,mira,input mux,output mux and memory are covered



It is the Top Module which consists of all the modules MBIST, MBIRA, IpMux, Main Memory (SRAM), Substitute Elements and OutMux. The MISR circuit has a scalable architecture, and it implements an enhanced version of ESP algorithm for efficient 2-D repair.The above Top module works in two modes- Test mode and Normal Mode. During RA, the MBIRA first records the unusable faulty substitute elements and then allocates substitute elements according to the faulty rows/columns of the main memory based on the test result. That is, the MBIST tests the substitute memory first to determine the available substitute elements then tests the main memory and simultaneously executes the RA process. For example, the sample 8 bit data inputted to Top module for write operation, like 8'hDE is given to AddrIn=3'h0; 8'h56 is given to AddrIn=3'h1; 8'hAD is given to AddrIn=3'h2; 8'h92is given to AddrIn=3'h5; 8'hAB is given to AddrIn=3'h6.The main memory has incurred faults due to coupling or adjacent or stuck at faults in certain locations like, FAddr=3’h2 whose faulty data is FData=8’h22; FAddr=3’h5 whose faulty data is FData=8’h44; FAddr=3’h6 whose faulty data is FData=8’h12. The BIRA module remaps the faulty memory locations to Substitute Memory address registers, thus eliminates writing the data on to faulty locations in main memory and enhances speed of memory access. During read operation, the faults which takes place in corresponding memory locations are remapped to substitute memory addresses like Substitute memory addr1=3’h2,Substituteaddr2=3’h5Substitute memory addr3=3’h6 and the input data is assigned to substitute memory registers by using BIRA circuit. Now the output is selected through the output multiplexer. If the circuit is fault free, the normal data is selected from the main memory address, whereas for the faulty memory the output is selected from the substitute memory address registers.

Conclusion

The Architecture gives a cost-effective MISR generator which enhances the MBIST generator with repair option for general embedded memories. It generated synthesizable RTL MISR circuits with little area overhead and high repair rate. The proposed MISR uses a memory substitute generated from the same memory generator as for the main memory without any implicit redundancy. It enhanced the EP RA algorithm for traditional 2-D or block redundancy repair with the proposed pivotal or configurable memory substitute’s architecture, which can allocate the memory substitute elements in row, column, or any block/rectangular patterns that the address bits can define. It also removed the memory substitute allocation phase of EP for lower area overhead and shorter analysis time.

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